CLAIMS

What is claimed is:

1. A method of forming a layer comprising a line and space pattern over a substrate including a first region and a second region, the method comprising the steps of:

depositing and patterning a first hard mask layer over the layer to form a master line and space pattern therein,

wherein a first master line and space pattern in the hard mask layer includes at least one line and at least one space of a minimum dimension dictated by a resolution limit of lithography;

etching the layer to form the line and space pattern in the second region corresponding to the first master line and space pattern in the hard mask layer in the second region,

wherein a line in the second region includes a first critical dimension (**B**) achievable at the resolution limit of lithography;

depositing a second hard mask layer over the patterned first hard mask layer,

etching the second hard mask layer to form sidewall spacers on sidewalls of at the least one line in the hard mask layer in the first region,

wherein the minimum dimension of the at least one space in the first hard mask layer in the first region is reduced to a second critical dimension (**A**) less than achievable at the resolution limit of lithography;

to form sidewall spacers on sidewalls of the at least one line in the second region; and

etching the layer to form the line and space pattern in the first region corresponding to the first master line and space pattern in the hard mask layer in the first region,

wherein a space in the first region includes the second critical dimension (**A**) less than achievable by the resolution limit of lithography.

2. The method according to claim 1, wherein the hard mask layer comprises at least one of silicon oxide, (Si_xO_y), silicon-dioxide (SiO_2), other oxides; silicon nitride (Si_xN_y), silicon rich nitride, oxygen rich nitride, other nitrides; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous or nanocrystalline form; and mixtures thereof.

3. The method according to claim 1, wherein the layer includes at least one of silicon, germanium, silicon-germanium alloys, silicon-carbon alloys, silicon-germanium alloys containing carbon, and other conductive and semi-conductive materials; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous; amorphous, single crystal, polycrystalline, nanocrystalline form; and mixtures thereof.

4. The method according to claim 1, further comprising the steps of:

depositing an anti-reflective coating (ARC) on the first hard mask layer;

patterning the ARC and the first hard mask layer to form a second master line and space pattern therein, the second master line and space pattern includes lines and spaces including a minimum dimension achievable at the resolution limit of lithography; and

depositing the second hard mask layer over the second master line and space pattern.

5. The method according to claim 1, further comprising the steps of:

depositing, patterning and etching a first photosensitive layer to form lines and at least one space therebetween, the lines in the first photosensitive layer include vertical walls and the at least one space therebetween includes the minimum dimension (**B**) achievable at the resolution limit of lithography; and

forming a first hard mask by transferring to the first hard mask layer a first patterned image of the first photosensitive layer by anisotropically etching the first hard mask layer to form therein lines and at least one space,

the at least one space in the hard mask layer includes vertical walls and the minimum dimension (**B**) achievable at the resolution limit of lithography.

6. The method according to claim 5, wherein the first photosensitive layer comprises photoresist.

7. The method according to claim 5, further comprising the steps of:

depositing, patterning and etching a second photosensitive layer over the substrate to form a second patterned image therein, comprising:

masking the first region, and

exposing the second region; and

transferring to the layer the line and space pattern of an exposed portion of the first master line and space pattern of the first hard mask layer by anisotropically etching the layer to form at least one line therein in the second region,

wherein the at least one line in the layer in the second region includes substantially vertical walls and the second critical dimension (**B**).

8. The method according to claim 7, wherein the second photosensitive layer comprises a photoresist.

9. The method according to claim 1, wherein the layer comprises multiple layers.

10. The method according to claim 1, further comprising the steps of:

forming a dielectric layer over the substrate, and

forming the first hard mask layer over the dielectric layer,

wherein the dielectric layer includes:

a charge-trapping dielectric layer in the first region, and

a gate dielectric layer in the second region;

wherein the charge-trapping dielectric layer includes:

a tunneling layer,

a charge-trapping layer and

an insulating layer,

wherein the tunneling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunneling layer and the insulating layer is disposed over the charge-trapping layer.

11. The method according to claim 1, wherein the first region includes a core region and the second region includes a periphery region.

12. The method according to claim 11, wherein the line and space pattern in the layer forms a core gate in the core region and a periphery gate in the periphery region.

13. A method of patterning a layer on a substrate including a first region and a second region, the method comprising the steps of:

providing a substrate including the layer to be patterned interposed between the substrate and a first hard mask layer to be patterned;

coating the first hard mask layer to be patterned with a first photosensitive layer;

patterning and etching the first photosensitive layer to form a first patterned image including lines and at least one space, the lines in the first photosensitive layer and the at least one space include substantially vertical walls and include a minimum dimension (**B**) achievable at a resolution limit of lithography;

transferring to the first hard mask layer the first patterned image by anisotropically etching the first hard mask layer to form lines and at least one space, the lines and the at least one space in the first hard mask layer include substantially vertical walls and the minimum dimension (**B**) achievable at the resolution limit of lithography;

coating the first hard mask layer with a second photosensitive layer;

patterning and etching the second photosensitive layer to form a second patterned image including a mask over the first region and exposing the second region;

etching the layer in the second region to form a line and space pattern therein including at least one line in the second region including the critical dimension (**B**) achievable at the resolution limit of lithography;

depositing a conformal hard mask layer over the hard mask layer, exposed surfaces of the layer and exposed surfaces of the substrate;

forming sidewall spacers on the vertical walls of the lines of the first hard mask in the first region whereby the minimum dimension (**B**) of the at least one space in the first region is reduced;

forming sidewall spacers on the vertical walls of the at least one line in the second region;

coating the substrate with a third photosensitive layer;

patterning and etching the third photosensitive layer to form a third patterned image,

wherein the first region is exposed and a remaining portion of the third photosensitive layer acts as a mask in the second region;

etching the layer in the first region to form a line and space pattern,

wherein the at least one space in the layer in the first region includes a second critical dimension (**A**) less than achievable by the resolution limit of lithography.

14. A semiconductor device, comprising:

a semiconductor substrate including a first region, a second region and an active region;

a dielectric layer formed over the semiconductor substrate;

a conductive layer formed over the dielectric layer,

wherein the conductive layer includes:

a first pattern in the first region comprising lines and an opening, the opening includes a first critical dimension (**A**) less than achievable at a resolution limit of lithography, and

a second pattern in the second region comprising at least one line including a second critical dimension (**B**) achievable at a resolution limit of lithography; and

a sidewall spacer formed on a sidewall of the at least one line, the sidewall spacer being formed from a hard mask layer.

15. The semiconductor device according to claim 14, wherein the dielectric layer comprises at least one of silicon oxide (Si_xO_y), silicon-dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$), binary and tertiary metal oxides, other metal oxides; silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), other nitrides; zirconium silicate, hafnium silicate, other silicates; ferro electric material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, or nanocrystalline form; and mixtures thereof.

16. The semiconductor device according to claim 14, wherein the conductive layer comprises at least one of silicon, germanium, silicon-germanium alloys, silicon-carbon alloys, silicon-germanium alloys containing carbon, and other conductive and semi-conductive materials; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, nanocrystalline form; and mixtures thereof.

17. The semiconductor device according to claim 14, wherein the dielectric layer includes:

a charge-trapping dielectric layer in the first region interposed between the first pattern in the first region and the substrate; and

a gate dielectric layer in the second region interposed between the second pattern in the second region and the substrate.

18. The semiconductor device according to claim 17, wherein the gate dielectric layer comprises a multiple layer gate dielectric layer.

19. The semiconductor device according to claim 17, wherein the charge-trapping dielectric layer includes:

a tunneling layer;

a charge-trapping layer; and

an insulating layer,

wherein the tunneling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunneling layer and the insulating layer is disposed over the charge-trapping layer.

20. The semiconductor device according to claim 14, wherein the dielectric layer includes a dielectric layer material including a permittivity greater than a permittivity of silicon-dioxide (SiO_2).